



Web Results 1 - 10 of about 161 for **"first counter" "second counter" "phase-locked loop" comparator error.** (0.68)

Digital phase locked loop circuit - Patent 4821293

A digital **phase locked loop** (PLL) circuit having an input terminal to which ... value and **second counter** means controlled by the output of said **comparator** ...

www.freepatentsonline.com/4821293.html

Single-chip DBS receiver - Patent 5953636

Hence, the **error rate** determined by the **comparator** provides a good ... At the same time the **second counter** is loaded, the **first counter** is also loaded with ...

www.freepatentsonline.com/5953636.html

EP0357527

The magnitude **comparator** compares the selected input interval value against the output ...

N is determined by the value in a **second counter**, N counter 16, ...

swpat.ffii.org/pikta/txt/ep/0357/527/

EP1116377

The output of switch 84 is input to a **first counter** 88 and the output of switch 86 is input to a **second counter** 90. Flip flop 80 is also coupled to a first ...

swpat.ffii.org/pikta/txt/ep/1116/377/

Discriminator or demodulator - Patent Storm

... may comprise a **comparator** 2 is typically provided. Any **error** is detected by finding a. ...

Device for frequency demodulation, using a **phase-locked loop**. ...

www.patentstorm.us/class/455/337-Discriminator_or_demodulator.html

Digitally controlled phase locked loop system - US Patent 4802009

... pulses of the signal provided by the **first counter**. The output signal of the **second counter** is the ... Plural distinct operating modes 375/376**Phase locked loop**. ...

www.patentstorm.us/patents/4802009.html

Frequency synthesizer using a wide-band voltage controlled ...

[0005] An integer-N **phase locked loop** (PLL) has been widely used as a radio ... a **comparator**, which receives an output signal of the **first counter** and an ...

www.freshpatents.com/ Frequency-synthesizer-using-a-wide-band-voltage-controlled-oscillator-and-a-fast-ada...

Digital pll circuit patent

[0009] The frequency **comparator** 8 detects a frequency **error** between a reference clock ...

The frequency 25 **comparator** has a **first counter**, a **second counter**, ...

www.freshpatents.com/ Digital-pll-circuit-dt20060105ptan20060001464.php

[PDF] Frequency and Time - Their Measurement and Characterization

File Format: PDF/Adobe Acrobat - [View as HTML](#)

Alternatively, a **second counter** may be used to begin counting the same time. base when the **first counter** stops. The second approach is illustrated in Fig. ...

tf.nist.gov/timefreq/general/tn1337/Tn061.pdf

Sonet ds-n desynchronizer.

... The **phase locked loop** contains a digitally controlled linear ... steps of incrementing a **first counter** to produce ... clock, incrementing a **second counter** to produce ...

patent.tange.dk/ziki/EP/5/3/EP536464.html

Try your search again on [Google Book Search](#)

Google ►

Result Page: [1](#) [2](#) [3](#) [Next](#)

[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2006 Google



Web Results 1 - 10 of about 29 for **"first counter" "second counter" "phase-locked loop" comparator "error detection"**

Method and apparatus for verifying a signal recorded in an encoded ...
an **error detection** circuit for comparing each of the second signal read out by ... 9i and
sends the count to a **comparator** 57. The **comparator** 57 compares the ...
www.freepatentsonline.com/5175655.html

Horizontal countdown system for television receivers - Patent 4335403
A system as set forth in claim 1 wherein said **phase locked loop** includes a ... the **error**
detection means includes means for sensing when the **second counter** ...
www.freepatentsonline.com/4335403.html

EP0096966

An A = B digital **comparator** circuit 40 includes a group of eight inputs ... **Error detection**
after the occurrence of the isolated ONE data bit and of the ...
swpat.ffii.org/pikta/txt/ep/0096/966/

EP0250661

17 is a schematic diagram of a chroma burst **phase-locked loop**; FIG. ... 25, including
error detection circuitry; FIG. 27 is a timing diagram for a clock ...
swpat.ffii.org/pikta/txt/ep/0250/661/

Plural active element (eg, triodes) - Patent Storm

a **comparator** of phase between a Digital Signal and a clock Signal adapted for the
construction of a **phase locked loop** in integrated circuit form, ...
[www.patentstorm.us/class/331/27-Plural_active_element_\(e_g_,_triodes\).html](http://www.patentstorm.us/class/331/27-Plural_active_element_(e_g_,_triodes).html)

Generation of a clock frequency in a smart card interface - US ...

said **phase locked loop** is a digitally operated **phase locked loop** responsive to a drive
clock signal, said arrangement further comprising a **second counter** ...
www.patentstorm.us/patents/5487084.html

United States Patent Application: 0040250180

the Input/output circuit of claim 5, wherein the clock **comparator** comprises: ... 63a supplies
error detection signal E1 to the **first counter** 64a when either ...
appft1.uspto.gov/.../20040250180&RS=DN/20040250180

Input/output circuit and semiconductor integrated circuit patent

The second EXOR circuit 63b supplies **error detection** signal E2 to the **second counter**
64b when either the second latch signal L2 or the third latch signal L3 ...
www.freshpatents.com/ Input-output-circuit-and-semiconductor-integrated-circuit-dt20041209ptan20040250180.php

Encoding unit and storage unit using the same US Patent 5673243

first counter means for counting the sum total of the logic values "1" in the pulse width
modulation data; **second counter** means for counting the sum total ...
patents.nimblewisdom.com/patent/ 5673243-Encoding-unit-and-storage-unit-using-the-same

EP312671 Ibm european software patent - Predictive clock recovery ...

the system includes a **first counter** N (20) which starts running in response ... This **second**
counter K is used to generate the extracted clock in phase with ...
gauss.ffii.org/ PatentView/EP312671

Try your search again on [Google Book Search](#)

Google ►

Result Page: [1](#) [2](#) [Next](#)

[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2006 Google

Basic Search

[Advanced Search](#) [Search Preferences](#)

"first counter" "second counter" "phase-locked loop"

Journal sources Preferred Web sources Other Web sources Exact phrase

Searched for:: :All of the words:"first counter" AND "second counter" AND "phase-locked loop" AND comparator

Found:: :5 total | 0 journal results | 4 preferred web results | 1 other web results

Sort by:: :relevance | date

Or refine:

All of the

1. DIGITAL PLL SYSTEM AND FAST FREQUENCY SWITCHING METHOD

ZUTA, Marc / ZUTA, Idan / ZUTA, Marc, PATENT COOPERATION TREATY APPLICATION, Nov 2000

...described at three levels: (1) a novel phase difference measuring unit capable of precise and fast phase measurement (2) a **phase-locked loop** PLL using the novel phase error measuring unit and other novel means and (3) a communication system using the novel PLL...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 4 results from Patent Offices](#)
[similar results](#)

2. Predictive clock recovery circuit

Abbate, Jean-Claude / Blanc, Alain / Jeanniot, Patrick / Lallemand, Eric / International Business Machines Corporation, EUROPEAN PATENT, Apr 1989
...stored into the **first counter** at second transition...which generates a **second counter** K that is expected...the value of the **first counter** N(i). This **second counter** K is used to generate...damping factor. A **comparator** comparing K(i) and...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 4 results from Patent Offices](#)
[similar results](#)

3. PNX15xx Series Data Book [PDF-3MB]

Dec 2004

PNX15xx Series Data Book Volume 1 of 1 Connected Media Processor Rev. 2 -- 1 December 2004 Philips Semiconductors PNX15xx Series Volume 1 of 1 Connected Media Processor 12NC 9397 750 14321 © Koninklijke Philips Electronics N.V. 2002-2003-2004. All rights reserved. Product data sheet Rev.

[http://www.semiconductors.philips.com/acrobat_download...]
[similar results](#)

4. TRIPLE MODULAR REDUNDANT COMPUTER SYSTEM

PETIVAN, James, L. / LUNDELL, Donald, C. / LUNDELL, Jonathan, K. / RESILIENCE CORPORATION, PATENT COOPERATION TREATY APPLICATION, Nov 1997
...oscillators 64A, 64B, 64C and respective **phase-locked loop** circuits 66A, 66B, 66C together with...the other modules. On each module, a **phase locked loop** circuit (PLL) compares a designated...is used by all three modules in the **phase-locked loop** process described above. That is...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 4 results from Patent Offices](#)

similar results

5. Method and apparatus for seismic geophysical exploration
Tims, Harold Arthur / Montgomery, Orin Carroll / Elliott, Sheldon Ellwood / Doggett, William Nance / PHILLIPS PETROLEUM COMPANY, EUROPEAN PATENT, May 1980
...system in which **error detection** and retransmission...system in which **error detection** and retransmission...the RF link. **Error detection** is utilized...schematic of a **first counter** illustrated...schematic of a **second counter** illustrated...
Full text available at patent office. For more in-depth searching go to  LexisNexis
[view all 4 results from Patent Offices](#)
similar results

fast :::

[Downloads](#) | [Subscribe to News Updates](#) | [User Feedback](#) | [Advertising](#)
[Tell A Friend](#) | [Terms Of Service](#) | [Privacy Policy](#) | [Legal](#)

[Powered by FAST](#) © Elsevier 2006

Basic Search

[Advanced Search](#) [Search Preferences](#)

"first counter" "second counter" "phase-locked loop"

Journal sources Preferred Web sources Other Web sources Exact phrase

Searched for:: :All of the words:"first counter" AND "second counter" AND "phase-locked loop" AND comparator

Found:: :52 total | 0 journal results | 51 preferred web results | 1 other web results

Sort by:: :relevance | date

Refine your search using these terms found in the patent abstracts

amplifier

clock pulses

control signal

decoder

decoding

error signal

frequency

frequency

output frequency

output signal

phase comparison

phase detection

phase error

reference signal

rising edge

waveform

Or refine search

All of the

1. PHASE-LOCKED LOOP CIRCUIT AND METHOD FOR CONTROLLING PHASE-LOCKED LOOP CIRCUIT

KUBOTA NORIMASA / TOSHIBA MICROELECTRONICS CORP, PATENT ABSTRACTS OF JAPAN, Sep 2005

...circuit 3, a **first counter** circuit 4...oscillator 9, a **second counter** circuit 10, a phase **comparator** 12 for receiving...I from the **second counter** circuit 10...J from the **first counter** circuit 4...converting a phase **error** signal L into...

Full text available at patent office. For more in-depth searching go to  LexisNexis® [view all 51 results from Patent Offices](#) [similar results](#)

2. Digital phase locked loop circuit

Hagiwara, Misao / NEC CORPORATION, EUROPEAN PATENT, Dec 1989

...relates to a **phase locked loop** (called hereinafter...a phase **comparator** and a control...signal. The **comparator** compares...that a phase **error** between the...discloses a **phase-locked loop** circuit for...comprising a **first counter** counting...signals, a **second counter** performing...

Full text available at patent office. For more in-depth searching go to  LexisNexis® [view all 51 results from Patent Offices](#) [similar results](#)

3. MULTI-MODE COMMUNICATIONS SYSTEM WITH EFFICIENT OSCILLATOR SYNCHRONIZATION

GARDNER, William, R. / QUALCOMM INCORPORATED, PATENT COOPERATION TREATY APPLICATION, Apr 2001

...includes a **first counter** that receives...implemented as a **phase-locked loop**, a direct...frequency. A **second counter** receives...required for the **first counter** to count...counted by a **second counter**. The second...provides an **error** signal in...

Full text available at patent office. For more in-depth searching go to  LexisNexis® [view all 51 results from Patent Offices](#) [similar results](#)

4. Improvements to digital phase-locked loop circuits

Mogavero Bruno, Carlo / Ambrosio, Renato / CSELT Centro Studi e Laboratori Telecomunicazioni S.p.A., EUROPEAN PATENT, Jul 1987

...to digital **phase-locked loop** circuits...signal, a **first counter** of the local...signal, a **second counter** of the local...decrement the **second counter**, in order...been the **phase-locked loop** (or PLL...The phase **comparator** determines...detected phase **error** is filtered...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 51 results from Patent Offices](#)
[similar results](#)

5. A COMMUNICATION SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A WIRELESS COMMUNICATION SYSTEM

KASAHARA, Masumi / OSAWA, Hirotaka / HENSHAW, Robert, Astle / TTPCOM LIMITED, PATENT COOPERATION TREATY APPLICATION, May 2003

...necessary to arrange **comparators** CMP1 to CMPn and...possible to dispose one **comparator**, one latch circuit...comparison by the **comparator**, and one exclusive...25 22 including a **first counter** 22N and a **second counter** 22A which further...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 51 results from Patent Offices](#)
[similar results](#)

6. Recording/reproducing apparatus

Niida, Mitsuo / Fujii, Akio / Ishii, Yoshiki / Hamanaka, Akiyoshi / Ohnishi, Shinji / CANON KABUSHIKI KAISHA, EUROPEAN PATENT, May 1996

...counter 6 counts this system clock to supply a new STC to the subtractor 2 to thereby constitute a feedback loop or a PLL (**Phase Locked Loop**). A time interval of SCR or PCR inputted to PLL is set to 700 msec or shorter for SCR and 100 msec or shorter for PCR...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 51 results from Patent Offices](#)
[similar results](#)

7. An apparatus and method for detecting field sync signals in a high definition television

Ki-Bum, Kim / Samsung Electronics Co., Ltd., EUROPEAN PATENT, Jul 1997

...output of a **first counter** Figure 5D...output of a **second counter** and Figure...frequency and **phase locked loop** (DFPLL) 108...correlator 206, a **comparator** 208, a latch 210, a **first counter** 212, a **second counter** 214, and...output of the **comparator** 208 according...to 0. The **second counter** 214 inputs...from the **first counter** 212 through...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 51 results from Patent Offices](#)
[similar results](#)

8. PAHSE LOCKED LOOP COMPRISING A VARIABLE DELAY AND A DISCRETE DELAY

BEESON, Peter / NOKIA CORPORATION, PATENT COOPERATION TREATY APPLICATION, Jul 2004

...Improved **Phase Locked Loop**. FIELD OF...a typical **phase locked loop** (PLL) 10...Thus the **first counter** produces...Thus the **second counter** provides...The adapted **phase locked loop** (PLL) 100...106 and the **first counter** 14, that...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 51 results from Patent Offices](#)
[similar results](#)

9. Plesiochronous demultiplexer

Wolf, Michael, Dr. / ALCATEL, EUROPEAN PATENT, Sep 2003

...or FEC (forward **error** correction) bytes...buffer, and a **comparator** for comparing...5 is fed to a **comparator** 6. The **comparator** 6 is connected...desynchronizer. A **first counter** 4 counts the write clock 13 and a **second counter** 5 counts the read...without inner **phase locked loop** control (PLL...

Full text available at patent office. For more in-depth searching go to  LexisNexis®
[view all 51 results from Patent Offices](#)
[similar results](#)

10. DIGITAL FREQUENCY SYNTHESIZER SYSTEM AND METHOD

ZUTA, Marc / ZUTA, Marc, PATENT COOPERATION TREATY APPLICATION, Oct 1998

...synthesizer, the lower is the Bit **Error** Rate (BER) of the communication...because of the quantization **error** and other effects. Frequency...than one cycle. To close the **phase locked loop**, the corresponding phase of...phase, and the resulting phase **error** applied to the VCO 3, as in...

Full text available at patent office. For more in-depth searching go to  LexisNexis®

[view all 51 results from Patent Offices](#)
[similar results](#)

11. Discriminator for differently modulated signals and method for reproducing original music data code

Jun, Ishii / Takashi, Tamaki / YAMAHA CORPORATION, EUROPEAN PATENT, Aug 2002

...is a block diagram showing the circuit configuration of a **comparator** incorporated in the wave discriminator Figs. 21 to 24 are...is a block diagram showing the circuit configuration of a **phase-locked loop** forming yet another part of the demodulator Fig. 41 is a...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

12. FREQUENCY SYNTHESIZER WITH PRESCALER

MACK, Michael, P. / MEHTA, Srenik / ATHEROS COMMUNICATIONS, INC., PATENT COOPERATION TREATY APPLICATION, Sep 2004

...controlled by a **phase locked loop** in which a dual...prescaler corrects an **error** introduced by...is based on the **first counter** output and the **second counter** output. The number...correcting the **error** introduced by...value. Thus' the **error** in the clock generated...state machine 504. **Comparator** 518 compares the...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

13. FREQUENCY LOCKED LOOP WITH DIGITAL OVERSAMPLING FEEDBACK CONTROL AND FILTER

TSYRGANOVICH, Anatoliy, V. / ZILOG INC., PATENT COOPERATION TREATY APPLICATION, Apr 2003

...leading edge **comparator** 184 from...trailing edge **comparator** 186, thus...i.e., a **first counter** 188, and a **second counter** 190) and two edge **comparators** 184, 186...provided to the **first counter** 188, whereas...provided to the **second counter** 190. In addition...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

14. NARROW BAND CHAOTIC FREQUENCY MODULATION USING SKEWED TENT MAPS

MOHAN, Chandra / ATLINKS USA, INC., PATENT COOPERATION TREATY APPLICATION, Feb 2003

...tent maps. The system includes a forward **error** correction encoder for receiving input...signal communication with the forward **error** correction encoder, a compression encoder...signal can be limited and detected with a **phase-locked loop** ("PLL") or a high-speed detector. Exemplary...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

15. A DIGITAL AUDIO RESOLVING APPARATUS AND METHOD

MOCK, Jeffrey, C. / AVID TECHNOLOGY, INC., PATENT COOPERATION TREATY APPLICATION, Oct 1997

...of the phase **comparator**. The output **error** signal in a typical **phase-locked loop** has a positive...generates an **error** signal to modify...without an analog **phase-locked loop** to overcome...includes a **first counter** that counts...first value, a **second counter** that counts...generates an **error** signal based...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

16. VOLTAGE CONTROLLED OSCILLATOR HAVING IMPROVED PHASE NOISE

BRETT, Stephen, Jonathan / STRANGE, Jonathan, Richard / FOWERS, Paul / JONES, Christopher, Geraint / ANALOG DEVICES, INC., PATENT COOPERATION

TREATY APPLICATION, Apr 2005

...the steps of determining an **error** between the oscillator amplitude...amplitude, and on the basis of the **error** measurement making a discrete...controlled oscillator within a **phase locked loop**, comprising a constant of...contributes to the loop gain of the **phase locked loop**, which controls the varactor...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

17. DIGITAL PLL SYSTEM AND FAST FREQUENCY SWITCHING METHOD

ZUTA, Marc / ZUTA, Idan / ZUTA, Marc, PATENT COOPERATION TREATY APPLICATION, Nov 2000

...synthesizer, the lower is the Bit **Error** Rate (BER) of the communication...because of the quantization **error** and other effects. Frequency...fast phase measurement (2) a **phase-locked loop** PLL using the novel phase **error** measuring unit and other novel...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

18. Timing signal generating circuit, semiconductor integrated circuit device and semiconductor integrated circuit system to...

Tamura, Hirotaka / Araki, Hisakatsu / Wakayama, Shigetoshi / Gotoh, Kohtaroh / Ogawa, Junji / FUJITSU LIMITED, EUROPEAN PATENT, Dec 1998

...and PLL (**Phase Locked Loop**) have been...include a **first counter** for counting...first clock a **second counter** for counting...value of the **second counter** reaches a...value. The **first counter** and the **second counter** may be loop...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

19. VCO frequency control circuit

Chung, Paul Wingshing / Gee, Ralph Leonard / Lang, Luke Chung Kuang / Saber, Paik / International Business Machines Corporation, EUROPEAN PATENT, Dec 1990

...VCO in a **phase-locked loop** (PLL). Background...Cycle-synchronised **phase-locked loop**" in IBM Technical...comprising: a **first counter** for counting...from the a **second counter** for counting...count in the **first counter** is stored...responsive to the **comparator** output signal...frequency **error** of the PLL...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

20. Predictive clock recovery circuit

Abbate, Jean-Claude / Blanc, Alain / Jeanniot, Patrick / Lallemand, Eric / International Business Machines Corporation, EUROPEAN PATENT, Apr 1989

...stored into the **first counter** at second transition...which generates a **second counter** K that is expected...the value of the **first counter** N(i). This **second counter** K is used to generate...damping factor. A **comparator** comparing K(i) and...

Full text available at patent office. For more in-depth searching go to  [LexisNexis](#)
[view all 51 results from Patent Offices](#)
[similar results](#)

fast :::

Results Pages: [[<< Prev](#)] [1](#) [2](#) [3](#) [[Next >>](#)]

[back to top](#)

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Sitemap](#)

Welcome United States Patent and Trademark Office

 Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORER GUIDE](#)[SUPPORT](#)

Results for "((first counter<in>metadata) <and> (second counter<in>metadata))<and> ..."

Your search matched **0** documents.A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order. [e-mail](#) [printer](#)**» Search Options**[View Session History](#)[New Search](#)**Modify Search** Check to search only within this results setDisplay Format: Citation Citation & Abstract**» Key****IEEE JNL** IEEE Journal or Magazine**IEE JNL** IEE Journal or Magazine**IEEE CNF** IEEE Conference Proceeding**IEE CNF** IEE Conference Proceeding**IEEE STD** IEEE Standard**No results were found.**

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.

[Help](#) [Contact Us](#) [Privacy & Security](#)

© Copyright 2006 IEEE - All Rights Reserved

Indexed by

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Sitemap](#)

Welcome United States Patent and Trademark Office

 Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORER GUIDE](#)[SUPPORT](#)

Results for "((first counter<in>metadata) <and> (second counter<in>metadata))<and> ..."
Your search matched 0 documents.

 [e-mail](#) [printer](#)

A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance in Descending order**.

» Search Options[View Session History](#)**Modify Search**[New Search](#) Check to search only within this results set**» Key**Display Format: Citation Citation & Abstract**IEEE JNL** IEEE Journal or Magazine**No results were found.****IEE JNL** IEE Journal or Magazine**IEEE CNF** IEEE Conference Proceeding

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.

IEE CNF IEE Conference Proceeding**IEEE STD** IEEE Standard[Help](#) [Contact Us](#) [Privacy & Security](#)

© Copyright 2006 IEEE – All Rights Reserved

Indexed by

PALM INTRANET

Day : Wednesday
Date: 3/29/2006
Time: 15:11:59

Inventor Information for 09/944500

Inventor Name	City	State/Country
HARTWELL, DAVID W.	BOSTON	MASSACHUSETTS

[Appn Info](#) [Contents](#) [Petition Info](#) [Atty/Agent Info](#) [Continuity Data](#) [Foreign Data](#) [Inven](#)

Search Another: Application# **or Patent#**
PCT / **/** **or PG PUBS #**
Attorney Docket #
Bar Code #

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | Home page


PALM INTRANET

Day : Wednesday

Date: 3/29/2006

Time: 15:12:03

Inventor Name Search Result

Your Search was:

Last Name = HARTWELL

First Name = DAVID

Application#	Patent#	Status	Date Filed	Title	Inventor Name
06040674	4244065	150	05/21/1979	WATER BED CONSTRUCTION	HARTWELL, DAVID
07606880	Not Issued	166	10/31/1990	REUSABLE CONTAINER	HARTWELL, DAVID
07860534	Not Issued	166	03/30/1992	MIS-SYNCHRONIZATION DETECTION SYSTEM	HARTWELL, DAVID
07870134	5301283	150	04/16/1992	DYNAMIC ARBITRATION FOR SYSTEM BUS CONTROL IN MULTIPROCESSOR DATA PROCESSING SYSTEM	HARTWELL, DAVID
07875564	Not Issued	161	04/27/1992	REUSABLE CONTAINER	HARTWELL, DAVID
08269234	6360285	150	06/30/1994	APPARATUS FOR DETERMINING MEMORY BANK AVAILABILITY IN A COMPUTER SYSTEM	HARTWELL, DAVID
08382953	5544179	150	02/01/1995	MIS-SYNCHRONIZATION DETECTION SYSTEM USING A COMBINED ERROR CORRECTING AND CYCLE IDENTIFIER CODE	HARTWELL, DAVID
09651531	Not Issued	160	08/29/2000	Automated backplane cable connection identification system and method	HARTWELL, DAVID
09652459	6977979	150	08/31/2000	ENHANCED CLOCK FORWARDING DATA RECOVERY	HARTWELL, DAVID
09652494	6640272	150	08/31/2000	AUTOMATED BACKPLANE CABLE CONNECTION IDENTIFICATION SYSTEM AND METHOD	HARTWELL, DAVID
09652563	Not Issued	160	08/31/2000	Enhanced clock forwarding data recovery	HARTWELL, DAVID
09652645	6724850	150	08/31/2000	DETERMINISTIC HARDWARE BEHAVIOR BETWEEN MULTIPLE ASYNCHRONOUS CLOCK DOMAINS THROUGH THE NOVEL USE OF A PLL	HARTWELL, DAVID

<u>09652980</u>	<u>6629257</u>	150	08/31/2000	SYSTEM AND METHOD TO AUTOMATICALLY RESET AND INITIALIZE A CLOCKING SUBSYSTEM WITH RESET SIGNALING TECHINQUE	HARTWELL, DAVID
<u>10649523</u>	<u>6976184</u>	150	08/27/2003	CLOCK FORWARD INITIALIZATION AND RESET SIGNALING TECHNIQUE	HARTWELL, DAVID
<u>60229830</u>	Not Issued	159	08/31/2000	Symmetrical multiprocessor computer system	HARTWELL, DAVID
<u>09292658</u>	Not Issued	161	04/15/1999	GRAPHICAL NETWORK SEARCH ENVIRONMENT	HARTWELL, DAVID CHARLES
<u>09652391</u>	<u>6738836</u>	150	08/31/2000	SCALABLE EFFICIENT I/O PORT PROTOCOL	HARTWELL, DAVID W.
<u>09652644</u>	<u>6701387</u>	150	08/31/2000	ADAPTIVE DATA FETCH PREDICTION ALGORITHM	HARTWELL, DAVID W.
<u>09653643</u>	<u>6668335</u>	150	08/31/2000	SYSTEM FOR RECOVERING DATA IN A MULTIPROCESSOR SYSTEM COMPRISING A CONDUCTION PATH FOR EACH BIT BETWEEN PROCESSORS WHERE THE PATHS ARE GROUPED INTO SEPARATE BUNDLES ANDROUTED ALONG DIFFERENT PATHS	HARTWELL, DAVID W.
<u>09944500</u>	Not Issued	121	08/31/2001	Detection of added or missing forwarding data clock signals	HARTWELL, DAVID W.
<u>09944516</u>	<u>6920516</u>	150	08/31/2001	ANTI-STARVATION INTERRUPT PROTOCOL	HARTWELL, DAVID W.
<u>10068427</u>	<u>6826653</u>	150	02/06/2002	BLOCK DATA MOVER ADAPTED TO CONTAIN FAULTS IN A PARTITIONED MULTIPROCESSOR SYSTEM	HARTWELL, DAVID W.
<u>10677583</u>	Not Issued	30	10/02/2003	Scalable efficient I/O port protocol	HARTWELL, DAVID W.
<u>10750495</u>	Not Issued	30	12/31/2003	Restoring access to a failed data storage device in a redundant memory system	HARTWELL, DAVID W.
<u>07093476</u>	<u>4858234</u>	150	09/04/1987	METHOD AND APPARATUS FOR ERROR RECOVERY IN A MULTIBUS COMPUTER SYSTEM	HARTWELL, DAVID W.
<u>07093479</u>	<u>4979097</u>	150	09/04/1987	METHOD AND APPARATUS FOR INTERCONNECTING BUSSES IN A MULTIBUS COMPUTER SYSTEM	HARTWELL, DAVID W.
<u>07093480</u>	<u>4837767</u>	150	09/04/1987	BUS ADAPTER MODULE WITH IMPROVED ERROR RECOVERY IN A MULTIBUS COMPUTER	HARTWELL, DAVID W.

SYSTEM					
07093488	4864496	150	09/04/1987	BUS ADAPTER MODULE FOR INTERCONNECTING BUSSES IN A MULTIBUS COMPUTER SYSTEM	HARTWELL, DAVID W.
07435397	5088419	150	11/13/1989	TABLES	HARTWELL, DAVID W.
07765417	Not Issued	166	09/25/1991	MEMORY SUBSYSTEM INPUT QUEUE	HARTWELL, DAVID W.
07870436	Not Issued	166	04/16/1992	DYNAMIC ARBITRATION FOR SYSTEM BUS CONTROL IN MULTIPROCESSOR COMPUTER SYSTEM	HARTWELL, DAVID W.
07870448	5412788	150	04/16/1992	MEMORY BANK MANAGEMENT AND ARBITRATION IN MULTIPROCESSOR COMPUTER SYSTEM	HARTWELL, DAVID W.
08023033	Not Issued	166	02/24/1993	SYSTEM FOR INTERLEAVING MEMORY MODULES AND BANKS	HARTWELL, DAVID W.
08110634	Not Issued	166	08/23/1993	DYNAMIC ARBITRATION FOR SYSTEM BUS IN MULTIPROCESSOR COMPUTER SYSTEM	HARTWELL, DAVID W.
08219807	5388222	150	03/28/1994	MEMORY SUBSYSTEM COMMAND INPUT QUEUE HAVING STATUS LOCATIONS FOR RESOLVING CONFLICTS	HARTWELL, DAVID W.
08248032	Not Issued	161	05/24/1994	DYNAMIC ARBITRATION FOR SYSTEM BUS IN MULTIPROCESSOR COMPUTER SYSTEM	HARTWELL, DAVID W.
08270297	Not Issued	166	06/30/1994	DISTRIBUTED DATA BUS SEQUENCING FOR A SYSTEM BUS WITH SEPARATE ADDRESS AND DATA BUS PROTOCOLS	HARTWELL, DAVID W.
08590802	5666551	150	01/24/1996	DISTRIBUTED DATA BUS SEQUENCING FOR A SYSTEM BUS WITH SEPARATE ADDRESS AND DATA BUS PROTOCOLS	HARTWELL, DAVID W.
08687692	5652861	150	07/26/1996	METHOD OF MEMORY INTERLEAVING, AND MEMORY SYSTEMS INTERLEAVED THEREBY	HARTWELL, DAVID W.
08869610	6076129	150	06/06/1997	DISTRIBUTED DATA BUS SEQUENCING FOR A SYSTEM BUS WITH SEPARATE ADDRESS AND DATA BUS PROTOCOLS	HARTWELL, DAVID W.

Inventor Search Completed: No Records to Display.

Search Another: Inventor	Last Name	First Name
	<input type="text" value="HARTWELL"/>	<input type="text" value="DAVID"/>
		<input type="button" value="Search"/>

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)